REMARKS

Applicant appreciates the time taken by the Examiner to review Applicant's present application. This application has been carefully reviewed in light of the Official Action mailed May 17, 2007. Applicant has amended Claim 1, 7 and 23 and submits that no new matter has been added. Thus, Claims 1-5, 7-17, 19-23 remain pending. Applicant respectfully requests reconsideration and favorable action in this case.

Rejections under 35 U.S.C. § 103

Claims 1-5, 7-17, 19-21 and 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,855,735 ("Webb") in view of U.S. Patent No. 4,543,657 ("Wilkinson") and further in view of U.S. Patent No. 3,916,379 ("Dulaney"). Claim 22 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Webb, Wilkinson and Dulaney, and further in view of U.S. Patent No. 5,867,409 ("Nozuyama"). Applicant respectfully traverses these rejections.

In order to establish a prima facie case of obviousness, the Examiner should show: that the prior art references teach or suggest all of the claim limitations; that there is some apparent reason to modify or combine the references; and that there the combination of references has a reasonable expectation of success. Applicant respectfully submits that because the combination of Webb, Wilkinson and Dulaney does not teach each of the claim limitations and that the combination would not have a reasonable expectation of success a prima facie case of obviousness has not been made.

Claim 1 recites receiving one or more bits of synchronization data from a transmitter in a receiver of a communications link, wherein the synchronization data corresponds to at least one bit from a corresponding transmitter shift register; loading the one or more bits of synchronization data into a shift register in the receiver, wherein the receiver shift register has a feedback circuit; if the receiver shift register is filled with synchronization data, initiating synchronized operation of the receiver shift register with the corresponding transmitter shift register, wherein during synchronized operation, a bit sequence generated by the receiver shift register is compared to a received bit sequence to identify the occurrence of errors in a data transmission from the transmitter; and if the receiver shift register is not filled with synchronization data, shifting the loaded synchronization data and loading one or more additional bits of synchronization data into the receiver shift register. Claim 7 and 23 recites similar limitations

Thus, embodiments of the systems and methods disclosed in the present application may provide a way to synchronize the generation of a pseudorandom bit sequences in a transmitter with the generation of a pseudorandom bit sequences in a receiver. The pseudorandom bit sequences may then be used to verify transmissions between the transmitter and the receiver.

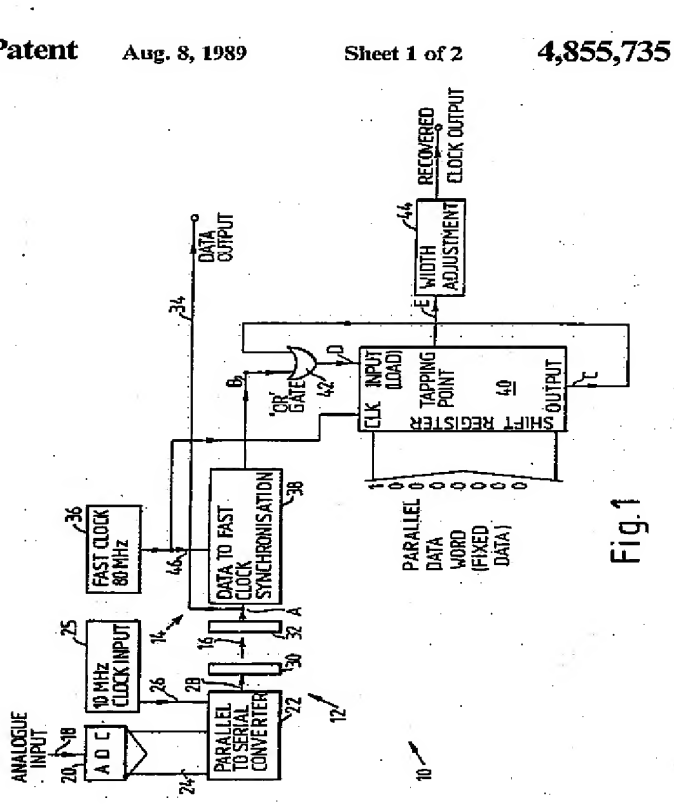
More specifically, in one embodiment, both the transmitter and the receiver have a linear feedback shift register (LSFR) which is operable to generate a pseudorandom bit sequence in the same way. In other words, if the same bit sequence is used in conjunction with the LSFR of the receiver and the LSFR of the transmitter the same pseudorandom bit sequence may be generated by both.

It is thus desired, in one embodiment, to synchronize the LSFR of the transmitter and the LSFR of the receiver such that both LSFRs generate the same pseudorandom bit sequence(s). To do this, synchronization data may be transmitted between the receiver and the transmitter. The synchronization data may comprise a first set of bits from the LSFR of the transmitter and sent to the receiver, where the first set of bits are put in the LSFR of the receiver. The LSFR of the transmitter may then generate another pseudorandom bit sequence, and a second set of bits from the LSFR of the transmitter may be sent to the receiver, where the second set of bits comes from the same location in (e.g. bits of) the LSFR of the transmitter as the first set of bits. The bits in the LSFR of the receiver are then shifted and the second set of bits placed in the LSFR in the same location (e.g. bits of) in which the first set of bits were placed. As described in more detail in the Specification at paragraphs [0043]-[0045] by operating in this manner, after a certain number of cycles the LSFR of the transmitter and the LSFR of the receiver may be synchronized and thus the LSFR of the receiver may generate a pseudorandom bit sequence(s) that are synchronized with the pseudorandom bit sequence(s) of the transmitter's LSFR. By transmitting a portion of a pseudorandom bit sequence generated by the LSFR of the transmitter to the receiver and comparing the portion of the pseudorandom bit sequence generated by the LSFR of the transmitter to the pseudorandom bit sequence generated by the LSFR of the receiver bit errors or a bit error rate may be determined.

Not All Limitations Disclosed

Webb, in contrast, discloses a method and system for the recovery of a data clock signal from a serial data stream. (*See,* Webb, Abstract, Summary) To explain the functionality

of Webb it may be useful to refer to Fig. 1 of Webb, reproduced below for the convenience of the Examiner:



Webb discloses a data sending station (12) and a data receiving station (14) connected via a radio frequency link (16). At data sending station (12) an analogue input is received at ADC (20) and converted to digital data, based upon clock signal (26) then, this data may be serialized for transmission to data receiving station (14). At receiving station (14), then, to accurately reconstruct the output of ADC 20 requires accurate recovery of the original data clock input (26). (*See,* Webb, Col. 4, Lines 1-15)

This is accomplished by a high speed clock (36), a synchronization circuit (38) which synchronizes the incoming data bits with the high speed clock (36), a recirculating shift register (40) and OR gate (42) connected to an input of the shift register (40). One input of the OR gate (42) receiving pulses from the synchronization circuit (38) and on line C from the shift register (40) output. The data clock recovered from the input signal is output from a tap point (E) of recirculating shift register (40). (*See,* Webb, Col. 4, Lines 15-25)

The synchronization circuit (38) is an edge triggered circuit connected to the high speed clock (36) and the received data stream (line A) such that the synchronization circuit (38) outputs a synchronized data pulse (on line B) whenever a leading edge of a one data bit is received. Each time one of these synchronized data pulses is received a parallel data word of fixed value 10000000 is loaded into the shift register (40) for recirculation. Because the shift register is (40) is 8 bits long and is being clocked at 8 times the rate of the original data clock (25) (which it is desired to derive) the original data clock (25) may be derived by tapping the recirculating shift register (40) at any one of the bits of the recirculating shift register (40) (e.g. line E). (*See,* Webb, Col. 4, Lines 1-40)

In other words, the value of 10000000 of eight bits is placed in, and circulated through, recirculating shift register (40) at eight times the rate of the original clock, resulting in a one being output from any location of the recirculating shift register (40) at 1/8 the pace of the high speed clock...or approximately the frequency of the original data clock (25).

Notice that the data sending station (12) of Webb does not have a shift register. Thus, 1) there is not a corresponding transmitter shift register in Webb, 2) the recirculating shift register (40) cannot be operated in synchronicity with a corresponding transmit shift register, 3) the data receiving station (14) of Webb cannot receive synchronization data from a transmitter where the synchronization data corresponds to one or more bits from a corresponding transmitter shift register, (4) such synchronization data is not loaded into the recirculating shift register (14) of Webb and finally, that 5) since no synchronization data is received from the data receiving station (14) of Webb, Webb does not load one or more additional bits of synchronization data into the recirculating shift register (14).

Consequently, Applicant respectfully submits that Webb does not disclose at least the limitations of Claim 1 which recite:

receiving one or more bits of synchronization data from a transmitter in a receiver of a communications link, wherein the synchronization data corresponds to at least one bit from a corresponding transmitter shift register,

loading the one or more bits of synchronization data into a shift register in the receiver, wherein the receiver shift register has a feedback circuit; if the receiver shift register is filled with synchronization data, initiating synchronized operation of the receiver shift register with the corresponding transmitter shift register, and

shifting the loaded synchronization data and loading one or more additional bits of synchronization data into the receiver shift register.

Consequently, Applicant respectfully submits that as Webb does not disclose at least the above limitations, the combination of Webb, Wilkinson and Dulaney does not disclose all the limitations of Claim 1.

Combination of Webb and Wilkinson Improper

As discussed above Webb utilizes a recirculating shift register (40), where the recirculating shift register (14) is operable upon the assertion of a signal to load a fixed value of 10000000 and to recirculate these values such that the output of the register may be provided as an input (e.g. to the register or OR gate (42). (*See,* Webb, Col. 3, Lines 10-20, Col. 4, Lines 1-30)

Wilkinson, in contrast, utilizes a pseudo-random number generator (PNG) which "are well known circuits which produce an apparently random series of encoded numbers up to a maximum number." (*See,* Wilkinson, Col. 2, Lines 2-6.)

Thus, the combination of the invention of Webb with the invention of Wilkinson would entail the use of the PNG of Wilkinson with the invention of Webb. However, the use of the PNG of Wilkinson with the invention of Webb would render Webb unsuitable for its intended purpose.

More specifically, the ability to generate the original data clock (25) at the tapping point (line E) of the recirculating shift register (14) of Webb depends on the specific characteristics of the recirculating shift register (14) described in Webb, namely that it is operable to be loaded with the value 10000000 and recirculate the value in the register such that the value output by the recirculating shift register (14) may be

provided as an input. If the PNG of Wilkinson were utilized in place of the recirculating shift register (14) of Webb, instead of the value of 1000000 being generated and the value within the register being circulated through the register at every cycle a pseudorandom number would be produced. As a pseudorandom number would be produced, a pseudorandom value would be provided at the tapping point (line E) of the recirculating shift register (14) of Webb. As the pseudorandom value being provided at the tapping point (line E) would almost certainly not be the same as the original data clock (25) of the data transmitting station (12), by using the PNG of Wilkinson the invention of Webb would be rendered unsuitable for its stated purpose of the "recovery of data clock signals from serial data streams." (*See,* Webb, Field of Invention).

As Webb would be rendered unsuitable for its intended purpose there would not be a reasonable expectation of success with respect to the combination of Webb and Wilkinson and similarly there would not be a reasonable expectation of success with respect to the combination of Webb, Wilkinson and Dulaney.

Accordingly, as the combination of Webb and Wilkinson and Dulaney does not disclose all the limitations of Claim 1 and the combination of Webb, Wilkinson and Dulaney would not have a reasonable expectation of success, Applicant believes that a case of obviousness has not been made with respect to Claim 1. Applicant therefore requests the withdrawal of the rejection of Claim 1 and similar Claims 7 and 23. Additionally, Applicant respectfully requests the withdrawal of the dependent Claims 2-5, 8-17 and 19-22 for at least the same reasons

Conclusion

Applicant has now made an earnest attempt to place this case in condition for allowance. Other than as explicitly set forth above, this reply does not include an acquiescence to statements, assertions, assumptions, conclusions, or any combination thereof in the Office Action. For the foregoing reasons and for other reasons clearly apparent, Applicant respectfully requests full allowance of Claims 1-5, 8-17 and 18-23. The Examiner is invited to telephone the undersigned at the number listed below for prompt action in the event any issues remain.

An extension of 2 month is requested and a Notification of Extension of Time Under 37 C.F.R. § 1.136 with the appropriate fee is enclosed herewith.

The Director of the U.S. Patent and Trademark Office is hereby authorized to charge any fees or credit any overpayments to Deposit Account No. 50-3183 of Sprinkle IP Law Group.

Respectfully submitted,

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Date: October 17, 2007

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